

A stable and low power on-chip system clock circuit for sensor nodes and low Power Timers

Aatmesh Shrivastava

Abstract- In this paper we present a $2\mu\text{W}$ temperature compensated on-chip digitally controlled oscillator and a 70nW uncompensated, ultra low power oscillator. The temperature compensated oscillator has a temperature stability of $8\text{ppm}/^\circ\text{C}$ while uncompensated oscillator has a stability of $4\%/^\circ\text{C}$. The uncompensated oscillator is calibrated using stable oscillator often to achieve high effective temperature stability. This combination gives us a stability of $8\text{ppm}/^\circ\text{C}$ @ 250nW if temperature changes by 1°C every second. A calibration scheme for the oscillator is also presented.

1. Introduction

In this paper we propose a low power on-chip oscillator with stability close to that of a crystal oscillator. The crystal oscillator [15] is used to generate the reference clock for almost all type of systems. The reference clock is usually multiplied many times using a phase locked loop (PLL) to generate the system clock. The ability of the crystal oscillator to provide an extremely stable clock is the primary reason for its choice. However a crystal oscillator consumes a significant amount of power and is costly. It is also not suited for the implantable platforms [26-27] because of the form factor as well.

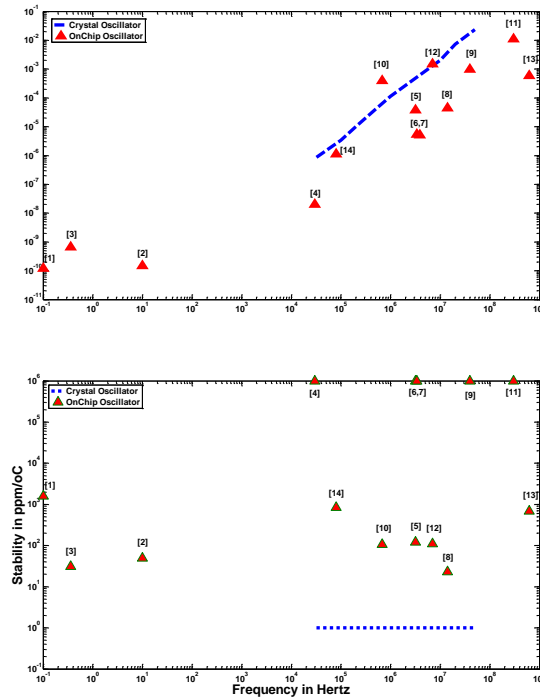


Figure 1 a)Power consumption b) temperature stability in crystal and on-chip oscillators

The power dissipated by a crystal oscillator can be a significant portion of the over-all system power particularly in the low power

space. There is a need to reduce this power in applications such as wireless sensor nodes (WSNs) which are now operating on harvested energy [21] with less than $10\mu\text{W}$ of power or for low power timers which operate all the time. There has been a recent trend to implement stable on-chip oscillators for applications such as wireless sensor nodes [25-26]. The key advantage of implementing an on-chip oscillator is much lower power as shown in Figure 1a). However, Figure 1b) shows that the temperature stability of crystal oscillator is at least two orders of magnitude better than the best reported on-chip oscillator [3] & [8]. The ideal solution would be an on-chip oscillator with temperature stability close to a crystal oscillator. In this paper we propose a scheme where the steady state power consumption of crystal oscillator can be eliminated and yet a very high accuracy clock signal can be retained.

The alternative clocking scheme for low power systems is an evolving field. Much emphasis is laid on reducing the power. There is also an opportunity to trade-off clock stability with power, therefore widely varied approaches exist [17-20]. In [17], Kellis proposes a hybrid clocking scheme employing a CMOS ring oscillator and an on-chip LC oscillator. Using the on chip ring and LC oscillator [17] results in a fast start-up and will provide good power savings particularly during wake-up of the system. Nevertheless, the clock will be unstable with the temperature. Also because of the aging of the CMOS process, oscillation frequency will keep on changing over-time. This kind of varying clock is difficult to integrate in a system design. In [18], Gundel presents $<20\mu\text{W}$ PLL designed to provide a clock frequency of 100KHz using a quartz reference of 32KHz . The reduced power level is achieved by carefully choosing the design components of PLL particularly voltage controlled oscillator (VCO). Here rather than a differential delay cell, a current-starved delay cell is used for VCO which has much lower power dissipation. Similarly in [19] the proposed scheme consumes around $200\mu\text{W}$. The authors of [20] presented an extremely low power clock reference circuit at ISSCC-2011. The scheme relies on the gate leakage current of a Zero Threshold voltage transistor (ZTVT) and a PMOS transistor. The gate leakage of a PMOS transistor increases with temperature (PTAT) while the gate leakage of ZTVT decreases with temperature (CTAT). These currents are added to get a temperature independent current. This scheme requires an additional transistor (ZTVT), which requires additional manufacturing steps and increases the cost. The scheme uses one-time calibration to account for process variation. It does not account for aging of the devices which can affect the output frequency. It obtains a frequency stability of $32\text{ppm}/^\circ\text{C}$. In our proposed scheme the frequency stability is less than $8\text{ppm}/^\circ\text{C}$ which can be compared to quartz oscillators and is better than ceramic oscillator [27]. The proposed oscillator consumes less $2\mu\text{W}$ of power operating at 200KHz . We then present a 70nW uncompensated oscillator running at 200KHz . We duty cycle these two oscillators to work out a desired stability-power point.

The paper is divided into following sections. In section 2 we discuss the oscillator architecture and its temperature

compensation scheme. In section 3 we explain process compensation effects. In section 4 we explain the calibration circuit. In section 5 temperature stability is presented, while in section 6 we present the low power DCO. Finally we present the results and conclusion in section 7 and 8.

2. Oscillator Architecture and Temperature Compensation

There are several ways in which an on-chip oscillator can be implemented. Often LC oscillators are used in RF applications. An LC oscillator has very high frequency selectivity [16], but it consumes a lot of area and power. An on-chip relaxation oscillator is another choice [8]. It usually incorporates couple of operational amplifier which makes it high area and high power design.

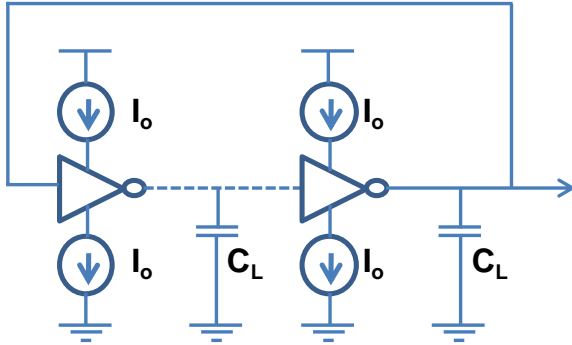


Figure 2 Current starved ring oscillator

The current starved ring oscillator is often considered better in terms of power and area [17-18]. The source of current can be different for different application needs. For example [1-3] gate leakage is used as current source. We chose this architecture because of its lower area and reduced power consumption.

Temperature compensation:

The frequency of oscillation of a current starved ring oscillator such as shown in Figure 2 is set by the current source I_o and load cap C_L . The capacitor usually implemented using metal-insulator-metal capacitor has very small temperature coefficient. Therefore, an oscillator with a frequency of oscillation independent of temperature, needs a current source independent of temperature. We obtain constant current source using the current from a MOS transistor and PTAT current source [23]. The current of a MOS transistor in strong inversion decreases with temperature (CTAT) as shown in Figure 3.

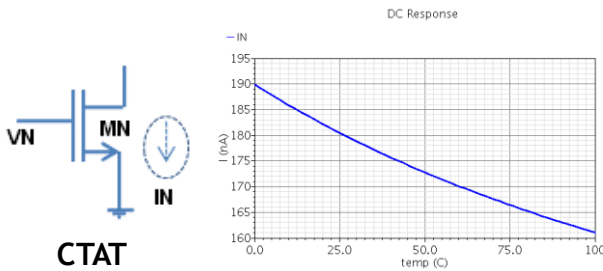


Figure 3 A MOS Transistor as CTAT current source

A current which increases with temperature (PTAT) can be generated using the circuit shown in Figure 4. We sum the current

of a PTAT and CTAT to obtain a constant current source shown in Figure 5.

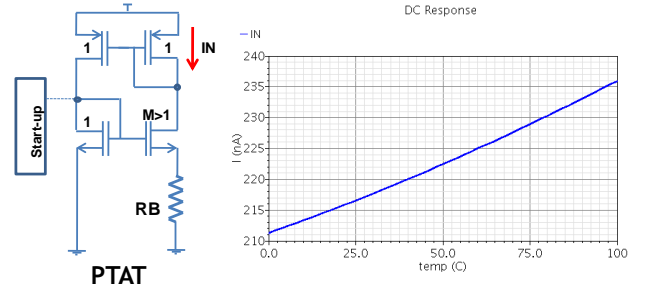


Figure 4 A PTAT current source

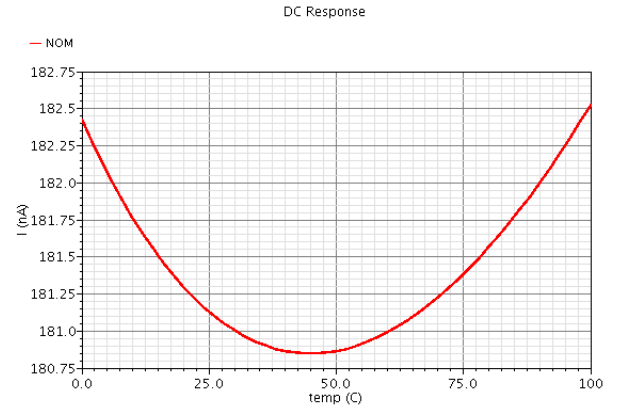


Figure 5 constant current with temperature

This current source has less than 1% variation with temperature. The use of this current source will result in very stable frequency of oscillation for our oscillator.

2nd order Temperature compensation:

The current source of shown in Figure 5 is used in our oscillator. It is quite stable with temperature. The delay through each delay element of the oscillator will not change with temperature to the first order. However it will still show a small variation with temperature in the 2nd order. We find that the delay through each element initially increases with the temperature (0-30°C) and then again start decreasing with the temperature (30-100°C). We implement a 2nd order compensation scheme to take care of later portion of temperature variation. It uses the leakage current.

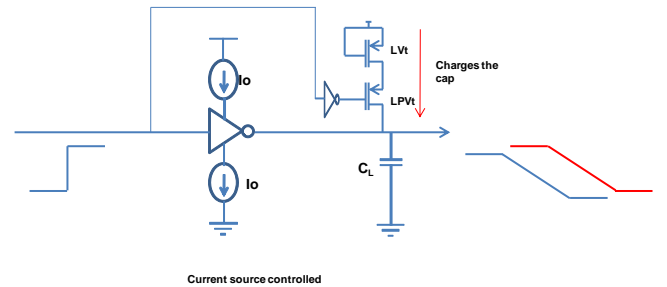


Figure 6 2nd order compensation scheme

The additional circuit comprises of an off, low threshold (LVT) transistor, a switch and an inverter. It essentially forms a pull-up path through leakage for the load capacitor C_L . This particular

portion of the circuit works when the delay element is pulling down. It works as follows. In the absence of this circuit the load capacitor C_L will discharge with the current I_o given by Figure 5. However, when this circuit is enabled the load capacitor will get some additional charge from the leakage of LVt transistor and so the delay through this delay element will increase slightly. This slight increase in delay increases with temperature. This nullifies the 2nd order increase in current at high temperature coming from the current source.

Using these techniques we obtain an oscillator whose output frequency has very small variation with temperature.

3. Process Compensation

The constant current source and the designed delay element will show change in behavior because of process variation. We employ process bits to compensate for the change in its behavior. The process compensation is applied on the current source and the 2nd order temperature compensation circuit using leakage current.

Current Source compensation:

The constant current source uses a PTAT and CTAT for its realization. The current from PTAT and CTAT current source will change with process. It is likely that one current may dominate over the other as process drifts. Therefore, the current source will either bend towards PTAT or CTAT depending on which current dominates. We compensate the current source by varying the resistance inside the PTAT

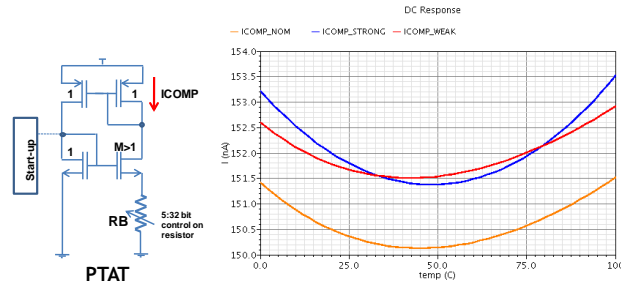


Figure 7 Process compensation of current source

Figure 7 shows the process compensation scheme and its results. We increase the resistance of the PTAT current source and decrease its current if the behavior of the constant current source is bent towards PTAT, similarly we decrease the resistance of the PTAT and increase its current if the constant current source comes out to be bent towards CTAT. A 5:32 binary decoder is used to achieve this. Figure 7 shows the constant current source with temperature at three different process corner points after bit compensation. It achieves constant current at each of these corners. So a constant current source with respect to temperature is obtained at irrespective of process variation. We employ similar calibration technique for 2nd order compensation using leakage current.

Global Mismatch:

We have shown that a constant current source can be obtained irrespective of the process variation. However, the absolute value of this current will change with process, as shown in Figure 6. The absolute value of the current source should also remain constant irrespective of the process to obtain a constant frequency output.

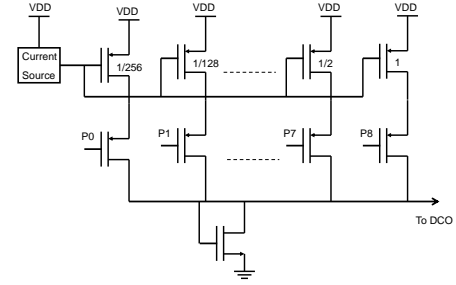


Figure 8 Binary weighted current source

We use binary weighted current mirror structure as shown in Figure 8. The constant current source forms the main current source whose binary weights are used to generate the desired current for a desired frequency.

Local Mismatch and frequency error:

The local mismatch and the digital nature of the binary weights used in the current source will produce small error in the desired frequency of oscillation. We use digital delay line made out of CMOS inverters to correct for these errors. We use 15 bit binary control on this delay line with 10 bit coarse and 5 bit fine control. This results in a Digitally Controlled Oscillator (DCO) as shown in Figure 8.

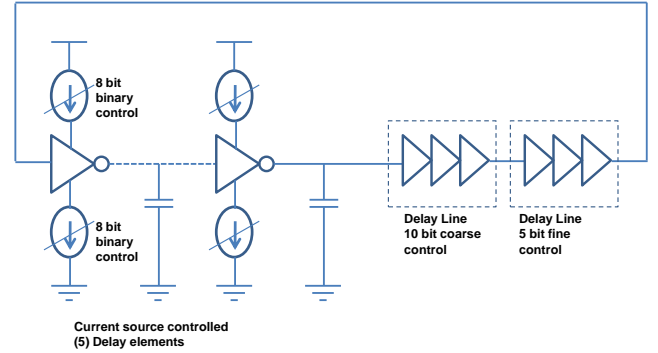


Figure 9 DCO structure

4. Calibration Technique

The proposed calibration circuit consists of a frequency comparator, SAR logic and the DCO in a feedback configuration as shown in Figure 10. The frequency comparator gives a high when DCO's output frequency is higher than reference and low when it is lower. The SAR logic approximates the current and delay inside the DCO based on the output of frequency comparator. There are overall 23-bit control on DCO. The first 8 bits are process control bits, which sets the large portion of the delay inside the DCO. The next bits are 10 bit coarse control which brings the resolution close 1nS. The fine bits can then bring resolution closer to 20pS.

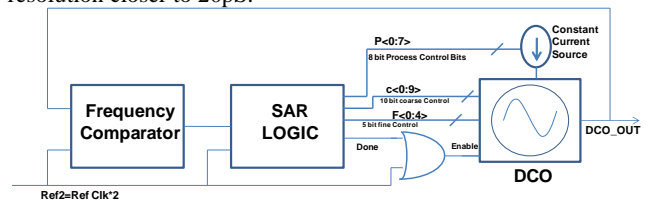


Figure 10 Calibration circuit for DCO using binary search

Frequency Comparator:

The frequency comparator is made of a 5-bit up counter and a register. The reference clock is divided by two and fed to the frequency comparator. We call the divided clock ref2. As the ref2 goes high the DCO gets enabled and will start oscillating. The counter is also enabled at the same time. The counter starts counting the rising edges of the DCO's output and is enabled for twice the time period of reference or the time at which ref2 is high. We know that output frequency of the DCO is higher than reference if counter has counted more than two else it is lower. This forms the basis of binary search using Successive approximation. The comparator out is registered on the falling edge of the ref2 which is provided to SAR logic to carry out the approximation when ref2 is low.

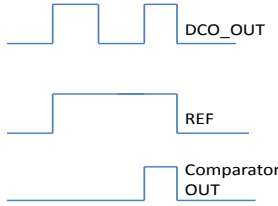


Figure 11 Timing Diagram of Frequency Comparator

SAR Logic:

The SAR logic block runs on the Successive Approximation Register (SAR) algorithm much like ADC and DAC systems. This algorithm is used to slowly converge on reference frequency. The DCO first assumes a frequency of half of its maximum output frequency. The SAR logic forces this value to the DCO. If the input frequency is greater than DCO's output frequency then the output at the frequency comparator will be a "1", else it will be a "0". The SAR logic then works to set this bit to the output of the comparator and then make an assumption about the following bit. This new bit string with the newly determined bit and new assumption gets passed to the DCO for the next approximation. The algorithm completes after the LSB has been determined. The DCO runs on its own once the bits are calibrated. The temperature compensation scheme keeps track of output frequency of DCO.

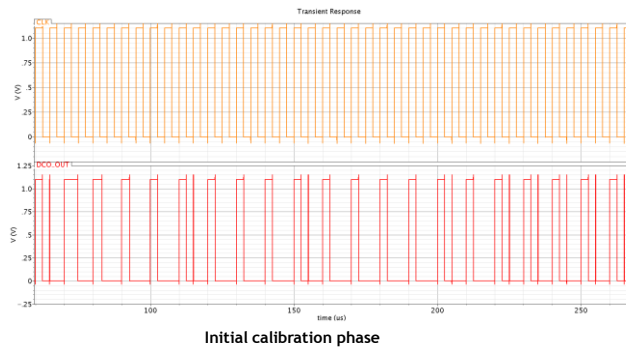


Figure 12 Transient response of DCO output and reference clock : Initial calibration

Figure 12 shows the transient behavior of the calibration circuit. It takes 46 reference cycles to get calibrated to reference frequency which is 200 KHz in this case.

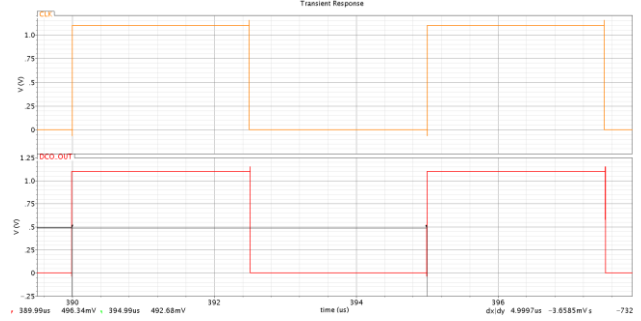


Figure 13 Final settled output

Figure 13 shows the output of the oscillator after calibration has happened. It shows a calibration error of 0.06%.

The proposed calibration has much simpler architecture than an ADPLL which causes it to have much lower settling time. It takes 46 cycles to settle compared to 64000 cycles in [22]. Consequently it consumes much lower power during calibration. After calibration it gives an output clock in phase with the reference. The proposed scheme does not keep the DCO in lock with the phase of reference clock as we intend to calibrate the DCO only one time because of its high temperature stability. However, one can keep the DCO locked to the reference using the counter control technique [23]. Here, the Stability of the oscillator controls the drift of the frequency.

5. Temperature Stability

We use the calibration scheme explained in the previous section to obtain the control bits for the DCO and calibrate it to run at 200 KHz at room temperature. After obtaining the calibration bits we run the DCO at different temperature and find its output frequency or period with respect to temperature variation.

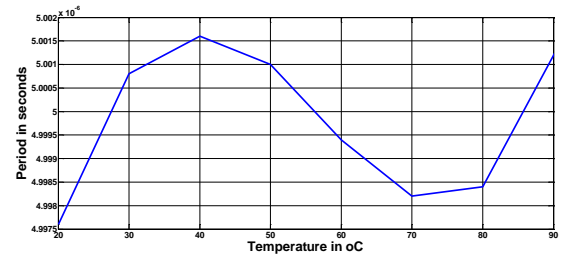


Figure 14 Temperature variation of clock period of DCO

Figure 12 shows the variation of output period of clock from 20°C to 90°C. The output period varies by 3nS over a temperature range of 70°C. This results in a frequency stability of 8ppm/°C.

6. Low Power DCO

In this section we present a low power DCO which uses leakage as its current source. We use this DCO for the case when temperature variation is not significant and save power.

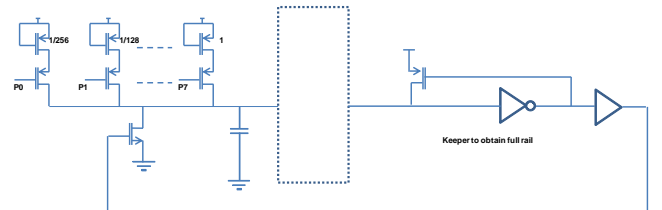


Figure 15 Leakage current based low power DCO

Figure 13 shows the DCO architecture. This architecture is similar to temperature compensated DCO described earlier. The current source here is replaced by binary weighted off LVt transistors. This saves power. It uses the same calibration scheme using frequency comparator shown in Figure 10. Similar digital inverter based coarse and fine delay lines are used to cancel mismatch effects. Figure 16 shows the transient response during calibration.

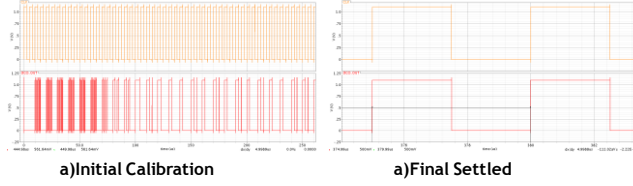


Figure 16 Transient response of DCO

The proposed low power DCO consumes 70nW of power at 200 Khz. The output frequency changes by 4% for a 1°C change of temperature which is equal to 40000ppm/ °C. We duty cycle this oscillator with stable oscillator to obtain desired stability power points.

7. Results

Figure 17 shows the results of proposed oscillator. We find that proposed oscillators have power in trend with the literature while we achieve stability 3 times better than the best reported work.

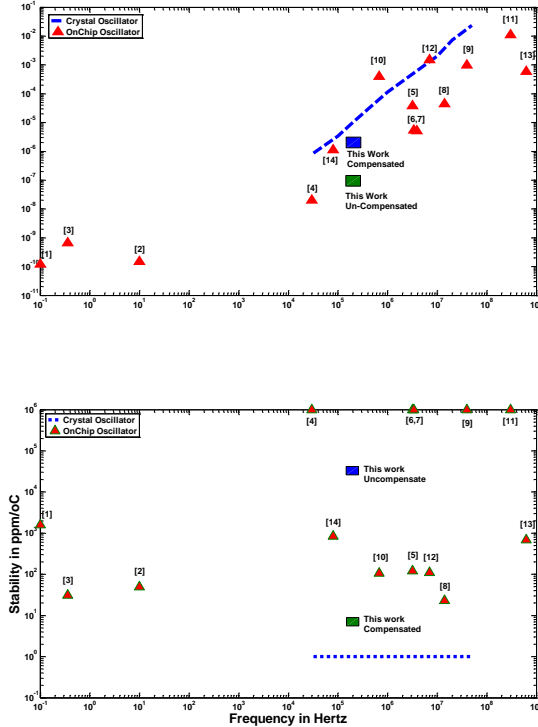


Figure 17 Power and stability of proposed Oscillator compared to recent work

Duty cycling between the two oscillators:

We calibrate the low power DCO with the accurate oscillator and then turn off the accurate oscillator. More often this is done more stable our system would with respect to temperature. This process

is called oscillator duty cycling. Figure 16 shows the power versus stability tradeoff for the two cases. In first case the temperature changes by 1°C in a minute and in second case, it changes by 1°C in a second. We find that in former the 8ppm/oC stability can be obtained at 75nW while in later it can be obtained at 250nW.

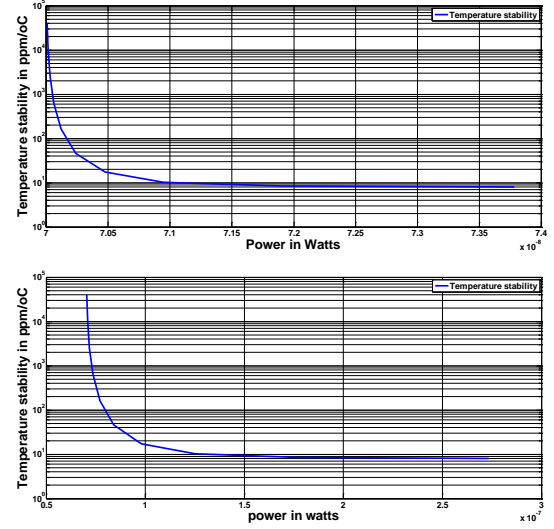


Figure 18 Power vs stability graph while duty-cycling the two oscillators when temperature changes by 1°C in a) a minute b) a Second

8. Summary

A very high stability 8ppm/oC oscillator is presented which can work as system clock. It gives in-phase output and employs very simple calibration circuit. It consumes less than 2uW of power. We have also presented a leakage current based ultra low power DCO. Low power DCO consumes 70nW. We further show that by duty-cycling the two oscillators, we can achieve stability of 8ppm/°C at 250nW if the temperature changes by 1°C every second

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